CLAIMS

What is claimed is:

1. A wafer holder for retaining a substrate within a processing chamber comprising:

an electrode; and

one or more layers covering a portion of the wafer holder in contact with the wafer where at least one of the layers is compliant.

2. The chuck of claim 1 wherein the compliant layer has a hardness between 25 and 100 Shore Hardness scale A.

3. The chuck of claim 1 wherein the compliant layer is an insulator having a dielectric constant between 1 and 3.

4. The chuck of claim 1 wherein the compliant layer can withstand 10% shear stress without exceeding the yield strength of the complaint layer material.

5. The chuck of claim 1 wherein the electrode comprises at least one conductive material selected from the group consisting of: copper, nickel, chromium, aluminum, iron, and mixtures or alloys thereof.

6. The chuck of claim 1 wherein the compliant layer comprises an insulative material selected from the group consisting of: fluorosilicones, polyamides, polyimides,

polyketones, polyetherketones, polysulfones, polycarbonates, polystyrenes, polyurethanes, nylons, polyvinylchlorides, polypropylenes, polyetherketones, polyethersulfones, polyethylene terephthalate, fluoroethylene propylene copolymers, cellulose, triacetates, silicones and rubbers, and combinations thereof.

7. The chuck of claim 1 wherein the compliant layer is between 1 and 3 μm thick.

8. An apparatus for projecting patterned charged particles onto a substrate comprising:

a processing chamber;

a charged particle source for generating a charged particle beam that impinges on the substrate; and

an electrostatic chuck comprising an electrode and one or more layers covering a portion of the wafer holder in contact with the wafer where at least one of the layers is compliant.

9. The apparatus of claim 8 wherein the compliant layer has a hardness between 25 and 100 Shore Hardness scale A.

10. The apparatus of claim 8 further comprising:

a computer for calculating an estimated charged particle beam deflection to compensate for the actual deformation of the substrate caused by the exposure of the

substrate to the charged particle beam, wherein the computer generates a deflection signal corresponding to the calculated deflection; and

a beam deflector for deflecting the charged particle beam in response to the deflection signal from the computer.

11. The apparatus of claim 8 wherein the compliant layer is an insulator having a dielectric constant between 1 and 3.

12. The apparatus of claim 8 wherein the compliant layer can withstand of 10% shear stress without exceeding the yield strength of the complaint layer material.

13. The apparatus of claim 8 wherein the electrode is comprises an conductive material selected from the group consisting of: copper, nickel, chromium, aluminum, iron, and mixtures or alloys thereof.

14. The apparatus of claim 8 wherein the compliant layer comprises an insulative material selected from the group consisting of: fluorosilicones, polyamides, polyimides, polyketones, polyetherketones, polysulfones, polycarbonates, polystyrenes, polyurethanes, nylons, polyvinylchlorides, polypropylenes, polyetherketones, polyethersulfones, polyethylene terephthalate, fluoroethaylene propylene copolymers, cellulose, triacetates, silicones and rubbers, and combinations thereof.

15. The apparatus of claim 8 further comprising:

a lithography mask positioned between the charged particle source and the substrate; and

an electron sensor disposed within the processing chamber for detecting backscattered electrons emanating from the substrate.

16. The apparatus of claim 8 further comprising a substrate temperature sensor for measuring the temperature of the substrate during processing and for sending a signal corresponding to the measured substrate temperature to the computer,

17. The apparatus of claim 8 wherein the compliant layer is between 1 and 10 μm thick.

18. The apparatus of claim 8 wherein localized heating of the substrate due to exposure to the charged beam is between 1° C and 50° C.

19. A method for patterning a photoresist layer on a substrate comprising the steps of:

forming a photoresist layer on the substrate;

positioning the substrate on an electrostatic chuck having one or more layers covering a portion of the wafer chuck in contact with the wafer where at least one of the layers is compliant; and

exposing portions of the photoresist layer on the substrate to a charged particle beam;

20. The method of claim 19 further comprising the steps:

computing an estimated deformation of the substrate caused by exposure of the substrate to the charged particle beam; and

deflecting the particle beam in response to the estimated deformation.

21. The method of claim 19 wherein the compliant layer has a hardness between 25 and 75 Shore Hardness scale A.

22. The method of claim 19 further comprising:

using a charged particle beam to scan a first mark on a photo lithography mask onto a second mark on said substrate;

detecting backscattered electrons from said scanning step;

determining the position of the substrate using the detected backscattered electrons; and

deflecting the charged particle beam in response to the measured position of the substrate.

23. The method of claim 19 wherein the compliant layer is an insulator having a dielectric constant between 1 and 3.

24. The method of claim 19 wherein the compliant layer comprises an insulative material selected from the group consisting of: fluorosilicones, polyamides, polyimides, polyketones, polyetherketones, polysulfones, polycarbonates, polystyrenes, polyurethanes, nylons, polyvinylchlorides, polypropylenes, polyetherketones, polyethersulfones, polyethylene terephthalate, fluoroethaylene propylene copolymers, cellulose, triacetates, silicones and rubbers, and combinations thereof.

25. The method of claim 19 wherein the exposing step is performed using a SCALPEL lithography system.

26. An electrostatic chuck for use in substrate processing, the chuck having an electrode covered by an insulative layer for receiving the substrate wherein the improvement comprises: the insulative layer which is elastic and can withstand 10% shear stress without exceeding the material yield strength.

27. The chuck of claim 26 wherein the compliant layer has a hardness between 25 and 100 Shore Hardness scale A.

28. The apparatus of claim 26 wherein the insulative layer comprises a material selected from the group consisting of: fluorosilicones, polyamides, polyimides, polyketones, polyetherketones, polysulfones, polycarbonates, polystyrenes,

polyurethanes, nylons, polyvinylchlorides, polypropylenes, polyetherketones, polyethersulfones, polyethylene terephthalate, fluoroethaylene propylene copolymers, cellulose, triacetates, silicones and rubbers, and combinations thereof.

29. A method for holding a wafer on a chuck having an electrode and one or more layers covering a portion of the wafer holder in contact with the wafer where at least one of the layers is compliant comprising the steps of:

placing the wafer on one of the layers of the chuck; and

energizing the electrode.

30. The method of claim 29 wherein the compliant layer has a hardness between 25 and 100 Shore Hardness scale A.

31. The method of claim 29 wherein the compliant layer is an insulator having a dielectric constant between 1 and 3.

32. The method of claim 29 wherein the compliant layer can withstand 10% shear stress without exceeding the yield strength of the complaint layer material.

33. The method of claim 29 wherein the electrode comprises at least one conductive material selected from the group consisting of: copper, nickel, chromium, aluminum, iron, and mixtures or alloys thereof.

34. The method of claim 29 wherein the compliant layer comprises an insulative material selected from the group consisting of: fluorosilicones, polyamides, polyimides, polyketones, polyetherketones, polysulfones, polycarbonates, polystyrenes, polyurethanes, nylons, polyvinylchlorides, polypropylenes, polyetherketones, polyethersulfones, polyethylene terephthalate, fluoroethylene propylene copolymers, cellulose, triacetates, silicones and rubbers, and combinations thereof.

35. The method of claim 29 wherein the compliant layer is between 1 and 10 μm thick.

36. An apparatus for handling a substrate for use in semiconductor processing comprising:

a wafer holder; and

one or more layers covering a portion of the wafer holder in contact with the wafer where at least one of the layers is compliant.

37. The apparatus of claim 36 wherein the compliant layer has a hardness between 25 and 100 Shore Hardness scale A.

38. The apparatus of claim 36 wherein the compliant layer can withstand 10% shear stress without exceeding the yield strength of the complaint layer material.

39. The apparatus of claim 36 wherein the compliant layer comprises an insulative material selected from the group consisting of: fluorosilicones, polyamides, polyimides, polyketones, polyetherketones, polysulfones, polycarbonates, polystyrenes, polyurethanes, nylons, polyvinylchlorides, polypropylenes, polyetherketones, polyethersulfones, polyethylene terephthalate, fluoroethylene propylene copolymers, cellulose, triacetates, silicones and rubbers, and combinations thereof.

40. The apparatus of claim 36 wherein the compliant layer is between 1 and 3 μm thick.